The Claims

The claims have not been amended, but are re-presented here for the convenience of the Examiner.

1. (previously presented) An apparatus, comprising:

a table to contain a plurality of entries, each entry including a frequency field and a voltage field; and

a register coupled to the table and having a selection field to select one of the plurality of entries;

wherein each of the entries is to indicate an operationally permissible combination of frequency and voltage.

2. (original) The apparatus of claim 1, wherein the register also has a limit field to specify how many entries are selectable.

3. (original) The apparatus of claim 2, wherein the selection field is a read-write field and the limit field is a read-only field.

4. (original) The apparatus of claim 1, wherein the frequency field includes a processor clock frequency indicator.

5. (original) The apparatus of claim 4, wherein the processor clock frequency indicator is a multiplier to be used with a phase locked loop circuit to generate a processor clock frequency.

6. (original) The apparatus of claim 1, wherein the voltage field includes a processor operating voltage identifier.

7. (original) The apparatus of claim 1, wherein the table is disposed in non-volatile memory.

8. (original) The apparatus of claim 7, wherein the table includes at least two entries.

9. (previously presented) A computer system, comprising:

a clock generator to selectively output a clock signal at any of a plurality of selectable processor clock frequencies;

a power supply to selectively output any of a plurality of selectable processor operating voltages;

a table coupled to the clock generator and the power supply and containing a plurality of entries, each entry including a frequency field and a voltage field; and

a register coupled to the table and having a selection field to select one of the plurality of entries;

wherein the entries are each to contain values in the frequency and voltage fields that represent an operationally permissible combination of frequency and voltage.

10. (original) The system of claim 9, wherein the register also has a limit field to specify how many entries are selectable.

11 (original) The system of claim 10, wherein the selection field is a read-write field and the limit field is a read-only field.

12. (original) The system of claim 9, wherein the frequency field includes a processor clock frequency indicator.

13. (original) The system of claim 12, wherein the processor clock frequency indicator is a multiplier to be used with a phase locked loop circuit to generate the processor clock frequency.

14. (original) The system of claim 9, wherein the voltage field includes a processor operating voltage identifier.

15. (original) The system of claim 9, wherein the table is disposed in non-volatile memory.

16. (original) The system of claim 15, wherein the table includes at least two entries.

17. (previously presented) A method, comprising:

writing into a selection field of a register;

using a content of the selection field to select one of a plurality of entries in a table, each entry having a frequency field and a voltage field containing indicators of operationally permissible values for frequency and voltage.

18. (original) The method of claim 17, wherein a content of the frequency field indicates a processor clock frequency.

19. (original) The method of claim 17, wherein a content of the voltage field identifies a processor operating voltage.

20. (original) The method of claim 17, further comprising:

using a content of a limit field in the register to determine how many entries are in the plurality of entries.

21. (original) The method of claim 17, further comprising:

using a content of the frequency field of the selected one of the plurality of entries to control an operating frequency of a processor clock.

22. (original) The method of claim 21, wherein using includes using the content of the frequency field as a multiplier to control an output frequency of a phase locked loop.

23. (original) The method of claim 17, further comprising:

using a content of the voltage field of the selected one of the plurality of entries to control an operating voltage to a processor.

24. (original) The method of claim 23, wherein using includes using the content of the voltage field to select from a plurality of operating voltages to the processor.

25. (original) The method of claim 17, wherein a content of the frequency field and a content of the voltage field in a selected entry of the table are matched to produce a combination of processor clock frequency and processor operating voltage that are operable in an associated processor.

26. (previously presented) A machine-readable medium having stored thereon instructions, which when executed by a processor cause said processor to perform:

determining a desired combination of processor clock frequency and processor operating voltage; and

writing to a register to select the desired combination of processor clock frequency and processor operating voltage from a table,

wherein each entry in the table contains values representing a pre-determined combination of frequency and voltage.

27. (original) The medium of claim 26, further comprising:

reading from the register to determine the current combination of processor clock frequency and processor operating voltage.

28. (original) The medium of claim 26, further comprising:

reading from the register to determine how many combinations of processor clock frequency and processor operating voltage are available to be selected.

29. (original) The medium of claim 26, wherein:

determining a desired combination is based on at least one of:

a performance goal;

a power consumption goal; and

operating characteristics of the processor.